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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,772	06/27/2003	Robert J. Royer JR.	884.905US1	6443

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EXAMINER	
PEIKARI, BEHZAD	

ART UNIT	PAPER NUMBER
2189	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/607,772	ROYER ET AL.	
	Examiner	Art Unit	
	B. James Peikari	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/18/07*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14-23* is/are rejected.

7)☒ Claim(s) *13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-4, 6-12, 14, 16, 19 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moran et al., (US Patent 5,359,713).

Moran et al. teach a method, comprising recording an address of a write operation to a memory cached by a non-volatile cache (note solid state non-volatile memory buffer 150, which acts a lower level of cache hierarchy between cache 161 and the main and mass memories 117A and 117B. Note columns 11 and 12). Moran et al. does not specifically mention that recording an address of a write operation should be done prior to executing an operating system cache driver. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made that this happens every time the computer 120 is booted or reset, because Moran explicitly states that one way of keeping track of access transactions (i.e., modifying data via writes, reads and erases) is by using an access transaction log. Note column 6, line 66, to column 7, line 14. By using such a log, the transactions and the addresses at which they occur are detected and recorded continuously at the time they occur so that if the system is *later* interrupted, reset or rebooted, and the boot drivers are initiated (including the cache drivers), such records in the log would have been made prior to boot, or else there would be no purpose in having such logs. The claims contain no additional limitation on the scope of "operating system cache driver", which is understood to be software from the operating system that is used to control the actions of the cache memory. Since, during the typical operation of cache memories, cache drivers are constantly being executed and cache memories are constantly be read and written to, it would have been obvious to one having ordinary skill in the art at the time the invention was made that a write to cache would occur before any next execution of the cache driver, in the system of Moran, since both operations were constantly

occurring in real time to keep the system running efficiently. Furthermore the claims contain no limitation whatsoever as to how long prior to executing an operating system cache driver the recording of the write address must occur. Thus, as a more extreme example, a write address could be recorded, the computer could be turned off and then turned on again a week later and this would be well within the scope of the claims.

As for the additional feature of invaliding the data corresponding to the address of the write operation, note column 18, lines 21-36.

As for the log also being stored in a non-volatile memory, note again column 6, line 66, to column 7, line 14.

14. Claims 5 and 17-18, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moran et al. (US Patent 5,359,713) in view of Lee et al. (US Patent 5,937,433).

As per claim 5, Moran et al. teach the method of claim 4 in the manner described above; however, Moran et al. do not teach that detecting the write operation further comprises trapping an interrupt request. Lee teaches the use of interrupt requests to detect write operations (Col 6, lines 6-8). The Lee and Moran et al. systems are compatible since they are in the same field of endeavor, namely cache control. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Lee with Moran et al. in order to properly detect write operations, since this would have been the proper handling of input/output requests in a computer system, and thus more efficient.

Lee further discloses the interrupt request is a basic input-output system int13h request (Col 6, lines 6-7).

16. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moran et al. (US Patent 5,359,713) in view of Heemels (US Patent 5,603,331).

As per claim 12, Moran et al. disclose the article of claim 10; but do not disclose the article wherein the data, when accessed, results in the machine performing setting a flag to indicate an overrun of the log. Heemels teaches setting a flag to indicate an overrun of the log (Col 9, lines 62-65). It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine Moran et al. with Heemels, adding the overfill flag of Heemels to the device of Moran et al. in order to provide for data integrity in the log. Heemels provides this motivation by indicating the flag would prevent the overrun of the log data array.

17. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moran et al. (US Patent 5,359,713) in view of the PC Guide.

As per claim 15, Moran et al. discloses the apparatus of claim 14; however he does not disclose that the address is a logical block address. According to a definition in PC Guide (Logical Block Addressing), LBA addressing is the dominant form of hard disk addressing. PC Guide shows that the motivation for using LBA is to allow for large hard disks that would otherwise not be supported by the BIOS. One of ordinary skill in the art would have found it obvious at the time the invention was made to combine Moran et al.

with the LBA definition in PC Guide in order to provide large hard disk compatibility for the apparatus of claim 14.

18. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moran et al. and Lee as applied to claim 20 above, and further in view of PC Guide.

As per claim 22, Moran et al. and Lee discloses the system of claim 20, but do not disclose that the module of claim 20 is included in a basic input-output system. According to PC Guide, (BIOS Functions and Operation), a basic input-output system handles interrupts. Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the module receiving interrupt requests associated with write operations into the BIOS.

Allowable Subject Matter

5. Claim 13 would be allowable if rewritten to include all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments filed with the response of January 18, 2007 have been fully considered but they are not deemed persuasive for at least the following reasons.

(A) With regard to the example of "a write address could be recorded, the computer could be turned off and then turned on again a week later and this would be well within the scope of the claims", applicant has not addressed this

argument at all based on its technical merits, but instead dismissed it as groundless supposition (i.e., personal knowledge). However, it is not simply personal knowledge. It is a clear example of what would teach the claims and it must be addressed by applicant, i.e., is it correct or is it incorrect?

(B) The claims contain no limitation on the scope of "operating system cache driver", which must be given its broadest reasonable interpretation. Operating system cache drivers are understood to be software from the operating system that is used to control the actions of the cache memory. During the typical operation of cache memories, cache drivers are constantly being executed and cache memories are constantly be read and written to, so it is very obvious that a write to cache would occur before, after and maybe during the execution of a cache driver, perhaps even several times a second.

(C) All of the arguments directed to the dependent claims hinge on the argument noted in section (A) above and thus are deemed to stand or fall with the independent claims.

(D) If applicant believes that a telephone interview would prove helpful, the examiner may be contacted at the number provided below.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Peikari whose telephone number is (571) 272-4185. The examiner is generally available between 7:00 am and 7:30 pm, EST, Monday through Wednesday, and between 5:30 am and 4:00 pm on Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon, can be reached at (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center at 866-217-9197 (toll-free).

B. James Peikari
Primary Examiner
Art Unit 2189
4/1/07